REMARKS

In the Office Action of November 28, 2003, claims 1-24 were presented for examination. Of these, claims 1-24 were rejected. Additionally, objections were made to certain claims and to Figure 3.

The status of the claims is now as follows:

Claims 1, 7, and 10 are amended. Claims 2, 6, 11 and 18 are cancelled without prejudice. Claim 25 is added.

Applicant will now address each point of the Office Action, in the order presented.

Objections

Claim 19 was objected to with the Examiner asking whether the "latch mode control signal" is the same as the "latch control signal." Applicant answers in the affirmative and corrects claim 19 above.

With respect to claim 20, the Examiner complains that certain claim language "seems a poor choice in wording." Applicant is unaware of any statute, rule of practice or case law that allows the Office to act as an editor and complain about wording choice. Applicant is entitled to be his own lexicographer and has done so in this instance, with the specification making it abundantly clear what is meant by the expression "participate in the shifting process." Thus, Applicant has considered the objection but believes it is unfounded and should be withdrawn. If the Examiner wishes to suggest language of equal scope, Applicant will consider a substitution.

With respect to Figure 3, the Examiner requests that it be designated as Prior Art. An appropriate amendment to Figure 3 is proposed herein.

With respect to claim 6, the objection is moot since claim 6 has been cancelled.

Anticipation by Imakura

The Office Action next rejects claims 1-9 under 35 USC 102(b) as anticipated by Imakura. In response, claim 1 has been amended to indicate, *inter alia*, that "the time required to convert the sequence of channels defined in the control word is proportional to the number of

channels selected by the user in the control word," and "wherein the N bit control word can be modified during the conversion of any one of the channels." By contrast, there does not appear to be any explicit disclosure in Imakura that the time taken to complete the conversion cycle varies according to the number of channels.

Imakura discloses an ADC which appears to allow a user-definable scan loop to be set up. We refer, for example, to Fig. 6. A scan selection flag register 9 has bits b0-b7 corresponding to inputs AN0-AN7. Additionally, a temporary scan sequence can be written into a temporary conversion request register 11 (column 8, lines 57-63). In the example given, bits b0, b1 and b2 are set so a scan loop AN0, AN1 and AN2 is formed. This loop is repeated until a stop command is issued. See column 9, lines 24-25. If the CPU controlling the ADC wants to temporarily include another value which has been preselected and loaded into the temporary register 11, then this temporary value, AN5, is also placed into the scan loop. The bits in the temporary conversion register are reset after a scan cycle has been completed. The embodiment of Fig. 8 is similar except that a counter is included such that the values in the temporary register are included for a number of scan cycles as counted by a counter 13. Nonetheless, there is no clear teaching that a short scan loop, such as AN0, AN1, AN2, as set out in Fig. 7, takes any less time than a longer scan loop such as AN0, AN1, AN2, AN5. Neither is there any discussion about taking elements out of the scan loop. Applicant cautions against conjecture.

Although with the benefit of hindsight, one might read into Imakura suggestions that the scan loop changes, the figures and detailed disclosure are not explicit and unambiguous and there is therefore no clear teaching and certainly no enabling disclosure concerning alteration of the time taken to complete the scan loop.

Consequently, there is no anticipation. The plainest reading of Imakura is that *each* of the bits in the scan selection flag register 9 is tested, and that irrespective of whether a bit is or is not set, the time taken to step from one bit in the register to the next bit in the register is *invariant*. Applicant believes that one skilled in the art would assume that the time to complete a scan cycle in Imakura was invariant of the number of channels, ensuring that changes in the number of selected channels did not result in changes in the time period between sampling

instance for a given channel. This provides some temporal certainty as to when a conversion has been performed which is of use when, for example, performing a Fourier transform.

Amended claim 1 includes features from original claims 1, 2 and 6, and draws out this distinction. It further provides that the control word can be modified during the conversion of any one of the channels, a feature not found in the reference.

The additional limitation added in claim 1 is supported by the specification at page 15, lines 18-21, in combination with page 16, lines 11-21 and Fig. 8, and the description relating thereto. It will be seen from Fig. 8 that the $\overline{CS}$ frames data conversion, and that the serial clock SCLK which drives the ADC core it ignored unless $\overline{CS}$ signal is low. Once the $\overline{CS}$ signal is low, programming data may be loaded in via the DIN pin, as set forth on page 17, lines 14-17. Thus, a 16-bit word can be written into the shadow register during any conversion, and this word controls the conversion sequence. See page 15, lines 18-21 and page 16, lines 11-16 which indicate that the content of the shadow register "will programme the sequence of channels to be converted on each successive valid $\overline{CS}$ falling edge."

Thus the present invention allows some or all channels to be selected or deselected at any point in the scan loop and the selection or deselection can be temporary or permanent. By contrast, can only add channels by the temporary conversion register, to those channels already selected in the scan selection register. It appears to be implied by Imakura that the scan selection flag register can only be over written once a scan loop has finished, since the presence of a temporary scan register would otherwise appear to be superfluous in many of the embodiments.

Consequently, the present invention offers the possibility of meeting a sudden request to select a new channel or combination of channels, whereas Imakura has a time overhead of needing to complete the scan sequence before being able to change it.

In view of the foregoing, the rejection of claims 1-9 should be withdrawn.

Obviousness (I)

Claims 10-15 and 17 have been rejected under 35 USC 103(a) as obvious over Imakura in view of Crocker et al and Jex et al, "and admitted prior art figure 3." Claims 10-15 and 17, we

initially note, depend, at least indirectly, from amended claim 1. The limitations of amended claim 1 discussed above as not being found in Imakura also are not found in the secondary references. Consequently, it is plain at the outset that the rejection is not supported and must be withdrawn.

Notwithstanding the foregoing, some additional comments are offered for the sake of completeness.

Notwithstanding the allowability of claim 10 based on the allowability of claim 1, claim 10 has been amended to include the limitations of claim 11, thereby making it clear that non-selected channels are bypassed. This combination is non-obvious over Imakura in combination with Crocker (putting aside for the moment Jex) because although Crocker shows counters that can be skipped within a ring counter, the choice of which counters to be skipped is hardwired so the user cannot freely determine which counters are to participate in the ring and which counters will not. This contrasts with the present invention wherein each individual one of the counters can either be arranged to participate or to be skipped. Consequently, claim 10 and all claims dependent thereon are patentable over Imakura and Crocker.

The Jex reference is irrelevant as there is no reason why a person of ordinary skill in the art would look to a "parallel synchronizer" in order to design an ADC, and the Examiner has not provided non-hindsight justification that one skilled in the ADC art would have looked to Jex.

None of the other references relate to an analog-to-digital converter. Thus, although the Examiner has found examples of ring counters where elements of the ring can be skipped, there is still no teaching or suggestion that it would be beneficial to vary the cycle time within an analog-to-digital converter; and the fact that doing so causes a variation in the sample time for measurements on any given channel may actually have led those skilled in the art away from such an idea.

Claims 10-15 and 17 are thus unobvious over Imakura in combination with Crocker and Jex.

Next, the Office Action rejects claim 16 as obvious over a combination of Imakura in view of Crocker and Jex and further in view of Widener. Widener is also inapposite and must be discounted because it discloses a circuit which can either clock on the rising edge or falling edge

of a clock pulse and hence does not disclose the functionality of the counter elements within the present invention where the counter can either participate in the ring or be effectively removed from the ring at the user's will. Moreover, Widener does not show a register acting as a buffer.

Anticipation-Crocker

Claims 18-23 are rejected as anticipated by Crocker. Claim 18 is canceled and reconsideration is requested as to claims 19-23. In particular, claim 19 relates to a latch where in the second mode of operation, the latch signal is transferred directly from the input of the latch to the output of the latch. This differs from Crocker, in which the skip circuit is built around the latches and by passes them. Consequently, the operation of a latch *per se* remains unaltered. Thus, in Crocker, latches D, E, and F are by passed, whereas in the equivalent circuit of the present invention, the latches would still be in the circuit but they would immediately propagate their inputs to their outputs. Claim 19 also differs from a D-type latch because typically a D-type latch (as, for example, described with respect to Figure 4 of the present application) propagates its input to its output on one stage of its clock and latches its input on another stage of its clock. Claim 19, on the other hand requires the presence of both the latch mode control signal and a latch signal, consequently requiring more signals to control it than does a simple D-type latch.

Therefore, upon reconsideration, claims 19-23 should be found allowable and the rejection should be withdrawn.

Obviousness (II)

Claim 24 has been rejected as obvious over Crocker in view of "admitted prior art figure 3." The Examiner's improper reading of claim 19 as anticipated by Crocker. In Jex, this rejection, as well, as claim 24 depends directly from claim 19. Having established that Crocker does not anticipate claim 19, and that the apparatus disclosed in Crocker, in fact, operates in a way that patentably differs from that described in claim 19, Crocker cannot, by itself, cures it own deficiencies and end up rendering obvious claim 24. Accordingly, the discussion above with respect to claims 19-23 makes the rejection of claim 24 improper, without further discussion being required.

Claim 25 is newly added. It is based upon Figure 4 and the description relating thereto and covers one of the latch circuits shown in Figure 4.

CONCLUSION

For the reasons expressed above, the claims remaining in the application are now all allowable over the references of record, taken singly or in combination, to the extent a combination is justifiable. Therefore, Applicant requests a Notice of Allowance. In the event the Examiner intends to further reject any claim, he is requested to first telephone the undersigned to attempt to resolve any remaining patentability issues.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,
Derek John Hummerston et al.

Steven J. Henry, Reg. No. 27,900
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210-2211
(617) 646-8000

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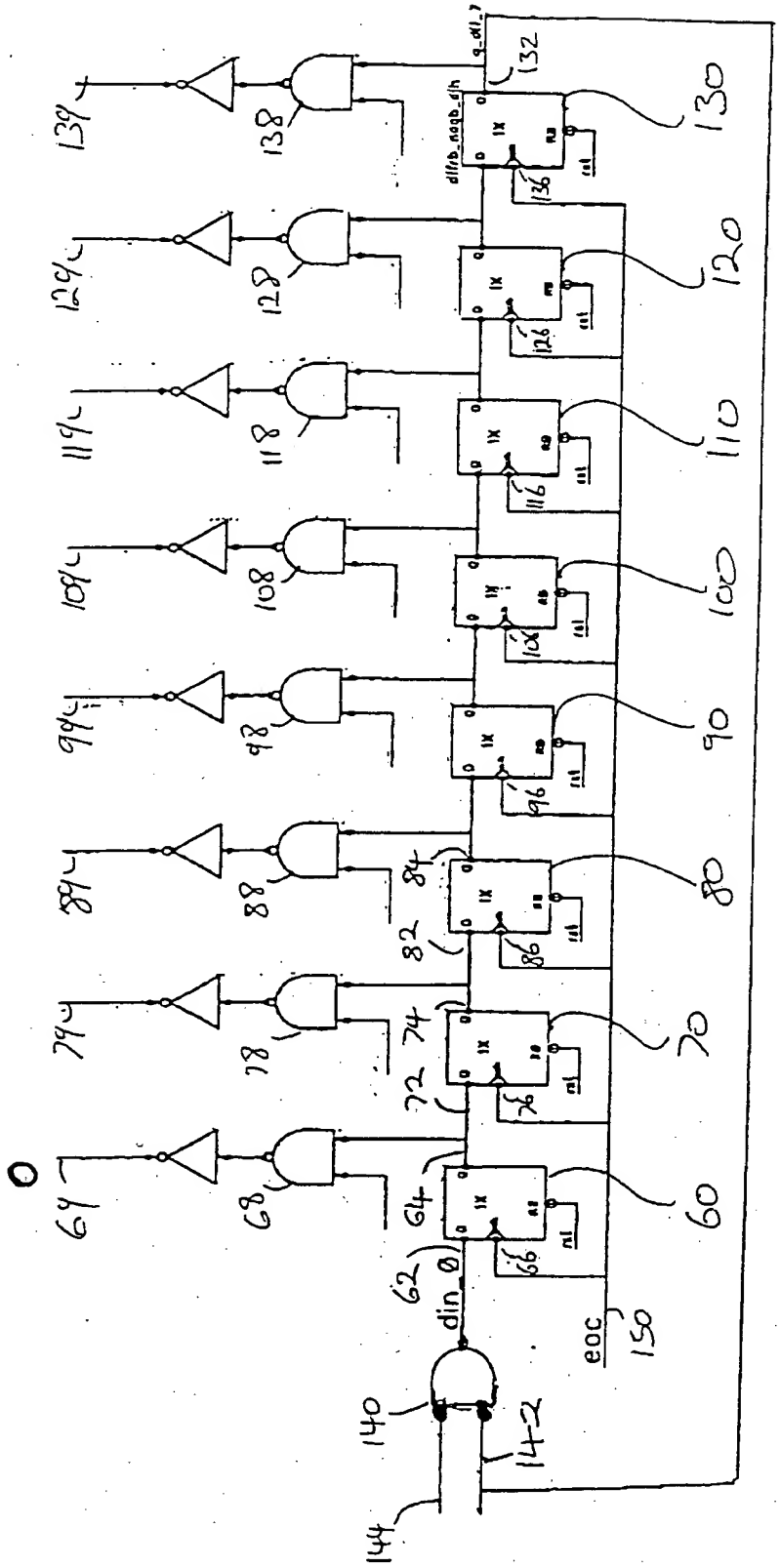

Fig 3

"PRIOR ART"